## Claims

[c1]

What is claimed is:

1.A method of forming a photo sensor in a photo diode formed on a semiconductor wafer, a surface of the semiconductor comprising a substrate with first-type dopants, and an insulating layer positioned on a surface of the substrate and surrounding the photo sensor, the method comprising:

performing a first ion implantation process utilizing second-type dopants to form a plurality of first doped regions on a surface of the photo sensor; and

performing a second ion implantation process utilizing second-type dopants to form a second doped region on the surface of the photo sensor, and the second doped region being overlapped with a partial region of each of the first doped regions.

[c2]

2.The method of claim 1 wherein the dopants in the first doped regions and in the second doped region interact with neighboring substrate to form a plurality of depletion regions.

[c3]

3.The method of claim 1 wherein the first-type dopants are N-type, and the second-type dopants are P-type.

[c4]

4.The method of claim 1 wherein the first-type dopants are P-type, and the second-type dopants are N-type.

[c5]

5.The method of claim 1 wherein the substrate further comprises an epitaxial silicon layer, and each of the first doped regions and the second doped region are formed inside the epitaxial silicon layer.

[c6]

6.The method of claim 1 wherein a dopant density of the first ion implantation process is less than a dopant density of the second ion implantation process.

[c7]

7.The method of claim 1 wherein the surface of the semiconductor wafer further comprises a logic circuit region, and the second ion implantation process forms at least a lightly doped drain (LDD) within the logic circuit region.

[c8]

8.The method of claim 1 wherein the method further comprises an annealing process for driving-in the dopants in the second doped region.

[c9]        9.The method of claim 1 wherein each of the depletion regions formed between
            the neighboring first doped regions is a complete depletion region, and a
            capacitance of each of the depletion regions is approximately equal to zero for
            increasing a sensing area, decreasing dark current, and further increasing photo
            current and photon conversion gain.

[c10]       10.The method of claim 1 wherein the second doped region is utilized to be a
            conducting wire of the photo sensor.

[c11]       11.A method of forming a photo sensor in a photo diode formed on a
            predetermined region of a P-type substrate of a semiconductor wafer, the
            predetermined region being surrounded by an insulating layer, the method
            comprising:
            performing a first ion implantation process to form a plurality of first N-type
            doped regions on a surface of the predetermined region; and
            performing a second ion implantation process to form a second N-type doped
            region on the surface of the predetermined region, and to form at least a lightly
            doped drain (LDD) on a surface of the semiconductor wafer outside the
            predetermined region.

[c12]       12.The method of claim 11 wherein the dopants in each of the first N-type
            doped regions and in the second N-type doped region interact with the
            neighboring P-type substrate to form a plurality of depletion regions.

[c13]       13.The method of claim 11 wherein the second N-type doped region is
            overlapped with a partial region of each of the first N-type doped regions.

[c14]       14.The method of claim 11 wherein the P-type substrate further comprises an
            epitaxial silicon layer, and each of the first N-type doped regions and the
            second N-type doped region are formed inside the epitaxial silicon layer.

[c15]       15.The method of claim 11 wherein a dopant density of the first ion
            implantation process is less than a dopant density of the second ion
            implantation process.

[c16]
            16.The method of claim 11 wherein the method further comprises an annealing

process for driving-in the dopants in the second N-type doped region.

[c17]     17.The method of claim 16 wherein each of the depletion regions formed
between the neighboring first N-type doped regions is a complete depletion
region, and a capacitance of each of the depletion regions is approximately
equal to zero for increasing a sensing area, decreasing dark current, and further
increasing photo current and photon conversion gain.

[c18]     18.The method of claim 11 wherein the second N-type doped region is utilized
to be a conducting wire of the photo sensor.

[c19]     19.The method of claim 11 wherein the lightly doped drain is positioned within
a logic circuit region.